DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:
My residence, post office address and citizenship are as stated next to my name.
I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled MULTI-CHIP WAFER LEVEL SYSTEM PACKAGES AND METHODS OF FORMING SAME, the specification of which (check one):

- ☐ is attached hereto.
- ☒ as filed on August 27, 2002 as United States application serial no. 10/229,914 and was amended on .
- ☐ as filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

			Priority	Claimed
(number)	(country)	(day/month/year filed)	Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available

DECLARATION FOR PATENT APPLICATION
(continuation page)

Invention Title: MULTI-CHIP WAFER LEVEL SYSTEM PACKAGES AND METHODS OF FORMING SAME

between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status–pending, patented or abandoned)
(application serial no.)	(filing date)	(status–pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

David V. Trask, Reg. No. 22,012
Laurence B. Bond, Reg. No. 30,549
James R. Duzan, Reg. No. 28,393
Allen C. Turner, Reg. No. 33,041
Kent S. Burningham, Reg. No. 30,453
Kevin K. Johanson, Reg. No. 38,506
Shawn G. Hansen, Reg. No. 42,627
Tawni L. Wilhelm, Reg. No. 47,456
Andrew F. Nilles, Reg. No. 47,825
Katherine A. Hamer, Reg. No. 47,628
Marcus S. Simon, Reg. No. 50,258
Trent N. Butcher, Reg. No. P-51,518
Michael L. Lynch, Reg. No. 30,871
William S. Britt, Reg. No. 20,969
Joseph A. Walkowski, Reg. No. 28,765
H. Dickson Burton, Reg. No. 48,396
Edgar R. Cataxinos, Reg. No. 39,931
Brick G. Power, Reg. No. 38,581
Krista Weber Powell, Reg. No. 47,867
Bretton L. Crockett, Reg. No. 44,632
Bradley B. Jensen, Reg. No. 46,801
Greg T. Warder, Reg. No. 50,208
Mardson Q. McQuay, Reg. No. P-52,020
Jeff M. Michelsen, Reg. No. 50,978
G. Scott Dorland, Reg. No. P-51,622
Charles B. Brantley II, Reg. No. 38,086

Address all correspondence to: Joseph A. Walkowski, telephone no. (801) 532-1922.

TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are

DECLARATION FOR PATENT APPLICATION
(continuation page)

Invention Title: MULTI-CHIP WAFER LEVEL SYSTEM PACKAGES AND METHODS OF FORMING SAME

punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first joint inventor: Swee Kwang Chua

Inventor's signature _____ Date 29-Oct-2002
Residence: Republic of Singapore
Citizenship: Republic of Singapore
Post Office Address: Blk 690, Hougang Street 61, #06-264, Singapore 530690

Full name of second joint inventor: Siu Waf Low

Inventor's signature _____ Date 29-oct-2002
Residence: Republic of Singapore
Citizenship: Malaysia
Post Office Address: 30, Lengkok Angsa, Singapore 239282

Full name of third joint inventor: Yong Poo Chia

Inventor's signature _____ Date 28 Oct 2002
Residence: Republic of Singapore
Citizenship: Republic of Singapore
Post Office Address: Blk 37, Bangkit Road, #10-03, Singapore 679976, Republic of Singapore

Full name of fourth joint inventor: Meow Koon Eng

Inventor's signature _____ Date 28 Oct 2002
Residence: Republic of Singapore
Citizenship: Republic of Singapore
Post Office Address: Blk 249, Pasir Ris St 21, #02-125, Singapore 510249

Full name of fifth joint inventor: Yong Loo Neo

Inventor's signature _____ Date 28 Oct 2002
Residence: Republic of Singapore
Citizenship: Republic of Singapore
Post Office Address: Blk 20, Upper Boon Keng Road, #07-1154, Singapore 380020

DECLARATION FOR PATENT APPLICATION
(continuation page)

Invention Title: MULTI-CHIP WAFER LEVEL SYSTEM PACKAGES AND METHODS OF FORMING SAME

Full name of sixth joint inventor: Suan Jeung Boon

Inventor's signature _____ Date 29 Oct 2002
Residence: Republic of Singapore
Citizenship: Republic of Singapore
Post Office Address: 271-A Jln Kayu, Singapore 799499

Full name of seventh joint inventor: Suangwu Huang

Inventor's signature _____ Date 29 Oct. 2002
Residence: Republic of Singapore
Citizenship: Republic of Singapore
Post Office Address: Blk 101, Jurong East St. 13, #07-170, Singapore 600101

Full name of eighth joint inventor: Wei Zhou

Inventor's signature _____ Date 29 Oct 2002
Residence: Republic of Singapore
Citizenship: Republic of Singapore
Post Office Address: Blk 263, Bukit Batok Ave 4, #07-255, Singapore 650263

Document in ProLaw